In the Specification:

Please replace the paragraph beginning on page 16, line 1 and ending on page 16, line 15 with the following amended paragraph:

Figure 8 is a diagrammatic representation showing one example of a system using secondary side arbitration, sometimes referred to as slave side arbitration, simultaneous multiple primary components, or simultaneous multiple masters. A system using individual arbitrators that correspond to individual secondary components accessible by more than one primary component is referred to herein as a secondary side arbitration system. The secondary side arbitration system no longer requires a bus or a system bus arbitrator that prevents a second primary component from accessing a second secondary component when a first primary component is accessing a first secondary component. According to various embodiments, a secondary component such as a memory 825 is associated with a secondary side arbitrator 851. However, secondary components UART 821 and PIO 823 are not associated with any arbitrator. In one example, secondary component UART 821 and secondary PIO 823 can only be accessed by primary CPU 813 and not by primary ~~Ethernet device~~ hardware accelerator 815. ~~A secondary~~ Secondary memory component 825, however, can be accessed by both primary CPU 813 and primary ~~Ethernet device~~ hardware accelerator 815.

Please replace the paragraph beginning on page 16, line 17 and ending on page 16, line 22 with the following amended paragraph:

According to various embodiments, a secondary side arbitrator 851 allows a first secondary component in a system to be accessed by a first primary component at the same time a second secondary component in the system is accessed by a second primary component. For example, ~~peripheral interface~~ memory 825 can be accessed by primary ~~Ethernet~~ hardware accelerator 815 through secondary side arbitrator 851 at the same time, secondary UART 821 is accessed by primary CPU 813.